REMARKS

The Examiner's Office Action of January 21, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

By the above actions, claim 1 has been amended and new claims 14 and 15 have been added. Claim 12 was cancelled previously, and claims 8-11 have been withdrawn from consideration. Accordingly, claims 1-7 and 13-15 are pending for consideration, of which claims 1 and 15 are independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 1-7 and 13 stand rejected under 35 U.S.C. §103(a) as unpatentable over Venkatesan et al. (U.S. Patent No. 6,326,301 – hereafter Venkatesan) in view of Admitted Prior Art (hereafter APA). This rejection is respectfully traversed at least for the reasons provided below.

As amended, claim 1 recites a semiconductor device comprising: a plurality of metal interconnects made from a multi-layer film composed of a first metal film (103) deposited on a semiconductor substrate (100) with an insulating film (101) sandwiched therebetween and a second metal film (105), which is a seed layer deposited on the first metal film (103); an interlayer insulating film (107) formed on the second metal film (105); and a via hole formed in the interlayer insulating film (107) and for exposing the second metal film (105), and a plug made from a third metal film (111) selectively grown on the second metal film (105) that is exposed at the bottom of the via hole, wherein the seed layer is laminated on the first metal film (103).

With respect to Venkatesan, the reference discloses that, as shown in Fig. 9, in a multilayer interconnect, an interlayer insulating film (18), which is a dielectric layer, is deposited on first metal films (14a, 14b), and a via (30, as shown in Fig. 8) is formed in the interlayer insulating film (18). Venkatesan also discloses that a second metal film (34), which is a seed layer, is in contact with the first metal films (14a, 14b) at the bottom of the via (30), and a plug made of third metal films (38a, 38b) is formed on the second metal film (34). However, the second metal film (34), which is a seed layer, is formed in the inner portion of the via (30) formed in the interlayer insulating film (18). In other words, the

second metal film (34) is formed within the interlayer insulating film (18) or on the interlayer insulating film (18).

On the other hand, the interlayer insulating film (e.g., 107) in the present invention is formed on the second metal film (e.g., 105), which is a seed layer. In other words, the second metal film (105) is formed below the interlayer insulating film.

According to Venkatesan, the second metal film (34), which is a seed layer, is formed within the interlayer insulating film (18), the second metal film (34) is not formed below the interlayer insulating film (18). Hence, Venkatesan, as well as APA, fails to disclose the feature of the present invention as recited in amended claim 1 of the present invention.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Venkatesan and APA cannot be applied, separately or in combination, in the §103(a) rejection because both fail to teach, disclose, or suggest a metal interconnect made from a multi-layer film composed of a first metal film deposited on a semiconductor substrate with an insulating film sandwiched therebetween and a second metal film, which is a seed layer deposited on said first metal film; an interlayer insulating film formed on said second metal film; a via hole formed in said interlayer insulating film and for exposing said second metal film; and a plug made from a third metal film selectively grown on said second metal film that is exposed at the bottom of said via hole, wherein said seed layer is laminated on said first metal film, as recited in amended claim 1.

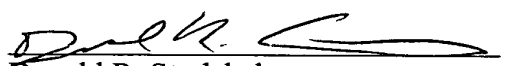
New claims 14 and 15 have been added to further complete the scope to which Applicants are entitled. Claim 15 parallels amended claim 1 but with the recital of a plurality of metal interconnects, a plurality of first metal films, and a plurality of second metal films.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending §103(a) rejection.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which

could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



Donald R. Studebaker
Registration No. 32,815

DRS/LCD

NIXON PEABODY LLP
Suite 900, 401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000